40Gbps QSFP+ 10KM LR4 SMF

Features

- Transmission data rate up to 11.2Gbps per channel
- QSFP+ MSA compliant
- Compliant to IEEE 802.3ba specification for 40GBASE-LR4 links
- 4 CWDM un-cooled DFB lasers, using ITU G.694.2 wavelength grid at 1270, 1290, 1310 and 1330nm
- High Sensitivity PIN-TIA with optical DEMUX
- Up to 10km reach over standard single mode fiber
- Compliant with QDR/DDR Infiniband data rates
- Hot pluggable electrical interface
- Lower power consumption
- Operating case temperature 0°C to +70°C
- 3.3V power supply
- RoHS 6 compliant (lead free)

Overview

The QSFP-40GFX13-D10 is a 4x10G hot pluggable optical transceiver. APC enables the integration of 4 transmitters, 4 receivers and an optical MUX/DeMUX into a small form factor package that delivers a 40Gbps data link in a compact QSFP footprint.

The optical connectivity is based on two SMF LC connectors, one for Tx and one for Rx. The Tx and Rx each consist of 4 10GB/s CWDM channels, whose wavelengths are in the 1300nm range. The QSFP-LR transceiver is designed for applications based on the IEEE 802.3ba 40BASE-LR4 standard of up to 10km reach.

Applications

- 40GBASE-LR4 40G Ethernet links
- Infiniband QDR and DDR interconnects
- Client-side 40G Telecom connections

Ordering Information

Part Number	Product Description
QSFP-40GFX13-D10	QSFP+ LR4 1270/1290/1310/1330nm 10km on Single mode Fiber (SMF)

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Functional Block Diagram

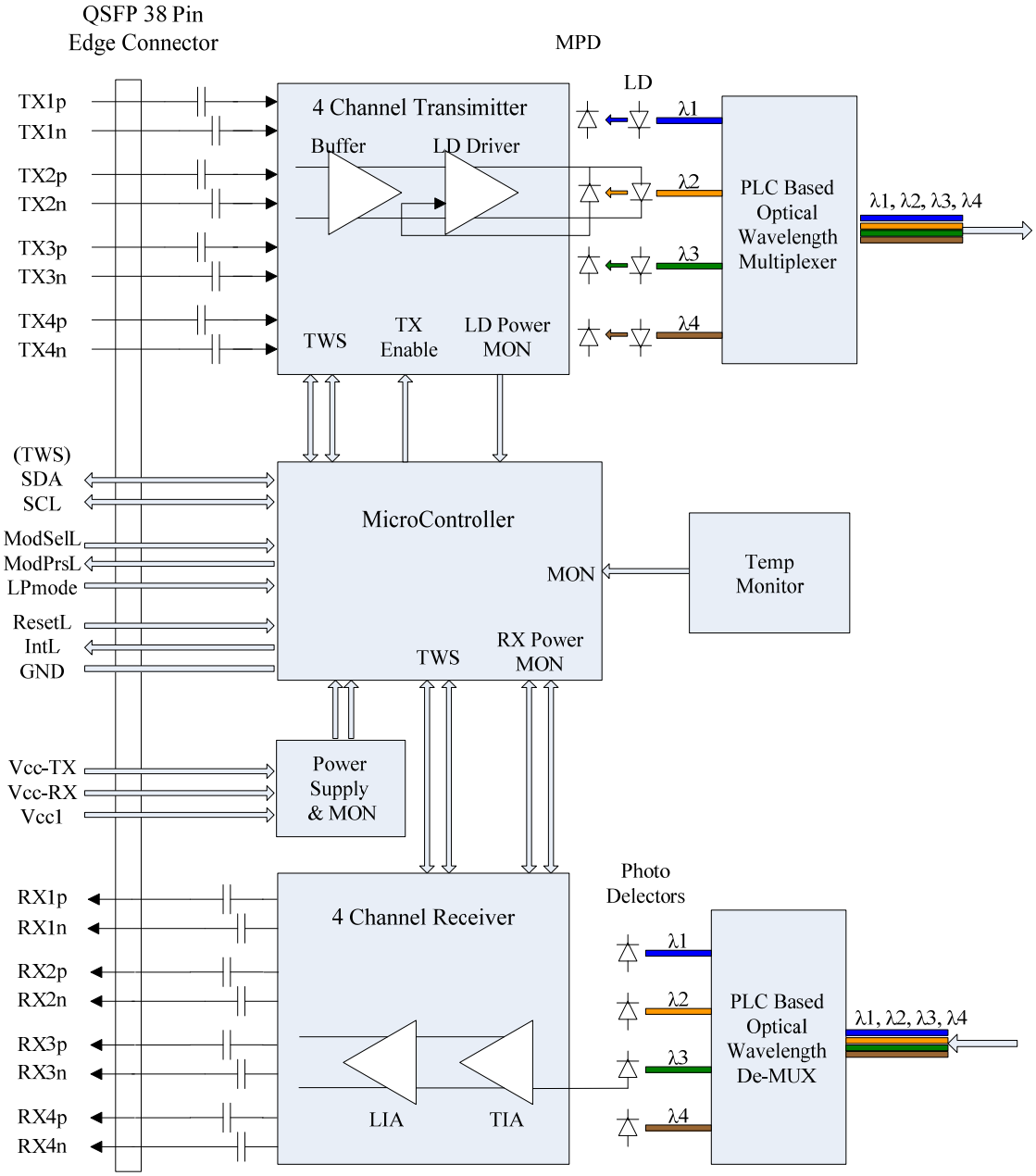

Figure1. Functional Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc-Tx Vcc-Rx Vcc1	0	3.6	V
Storage Temperature Range	T_{STG}	-40	+85	ºC
Maximum Average Input Optical Power per lane (Damage Threshold)	P_{IN}	3.3		dBm
Relative Humidity	RH	10％to 90％(non-condensing)		

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc-Tx Vcc-Rx Vcc1	3.1	3.5	V
Operating Case temperature	T_{CASE}	0	70	ºC
Power Consumption	P_{DISS}		3.5	W
SMF Link Length	L_{KM}		10	km

High Speed Electrical Specifications

Parameter	Min	Typical	Max	Units
General				
Supply Voltage	3.1	3.3	3.5	Volts
Supply Current			1.0	Amps
Maximum Power Consumption			3.5	Watts
Maximum Power Consumption – LP Mode			1.5	Watts
Signaling Speed Per Channel		10.3125		Gb/s
Signaling Speed Operating Range		±100		ppm
Transmitter				
Transmitter Differential Input Impedance		100		ohms
Transmitter Differential Input Voltage	0.2		1.6	Volts
Receiver				
Differential Output impedance		100		ohms
Differential output voltage		300	850	mV

Rise Time			60	ps
Fall Time			60	ps

Optical Characteristics

Transmitter Specifications – Optical

Parameter	Min	Typical	Max	Unit
Lane Wavelength Range	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm
Data Rate Per Lane		10.3125		Gb/s
Average Optical power per lane	-7		2.3	dBm
Total Average Launch power			8.3	dBm
Optical Modulation Amplitude (OMA), each lane	-4		3.5	dBm
Extinction Ratio	3.5			dB
Difference in launch power between any two lanes			6.5	dB
Relative Intensity Noise (RIN)			-128	dB/Hz
Launch Power in OMA minus TDP, each lane	-4.8			dBm
Transmitter and dispersion penalty (TDP), each lane			2.6	dB
Side-Mode Suppression Ratio (SMSR)	30			dB
Average Launch Power per lane @ TX off state			-30	dBm
Transmitter Reflectance			-12	dB
Optical return loss tolerance			20	dB
Transmitter Eye Mask definition: X1, X2, X3, Y1, Y2, Y3	Compliant with 802.3ba standard {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Eye Mask Criteria	5% mask margin over specified ranges of temperature, voltage and power supply noise at end of life.			

Receiver Specifications – Optical

Parameter	Min	Typical	Max	Unit
Lane Wavelength Range	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm

Damage Threshold				3.3	dBm
Average Receive Power, each lane		-13.7		2.3	dBm
Receive Power, each lane (OMA)				3.5	dBm
Difference in Receive Power between any two lanes (OMA)				7.5	dB
Receiver Reflectance				-26	dB
Receiver Sensitivity (OMA) per lane (10.3125Gb/s @ PRBS 2^{31}-1 and BER=10^{-12})				-11.5	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane				12.3	GHz
Stressed Receiver Sensitivity OMA), each lane				-9.6	dBm
Conditions of stressed receiver sensitivity tests	Vertical eye closure penalty, each lane	1.9			dB
	Stressed eye jitter per lane	0.3			UI

Receiver Output Power Thresholds for Loss of Signal (LOS)

Parameters	Min	Typical	Max	Unit
RX_LOS_Assert Min/Max (dBm)	-30		-20	dBm
RX_LOS_De-Assert Max(dBm)			-17	dBm
RX_LOS_Hysteresis (dBm)	0.5			dB

Recommended Host Board Power Supply Filtering

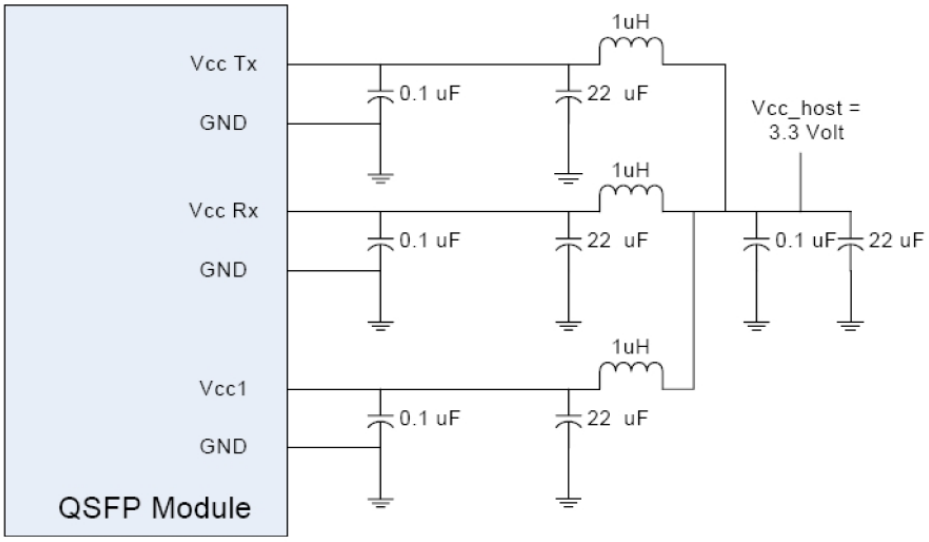

Figure2. QSFP voltage supply and filtering scheme

QSFP Edge Connector and Pinout Description

The electrical interface to the transceiver is a 38-pin edge connector. The 38-pins provide high speed data, low speed monitoring and control signals, I^2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.

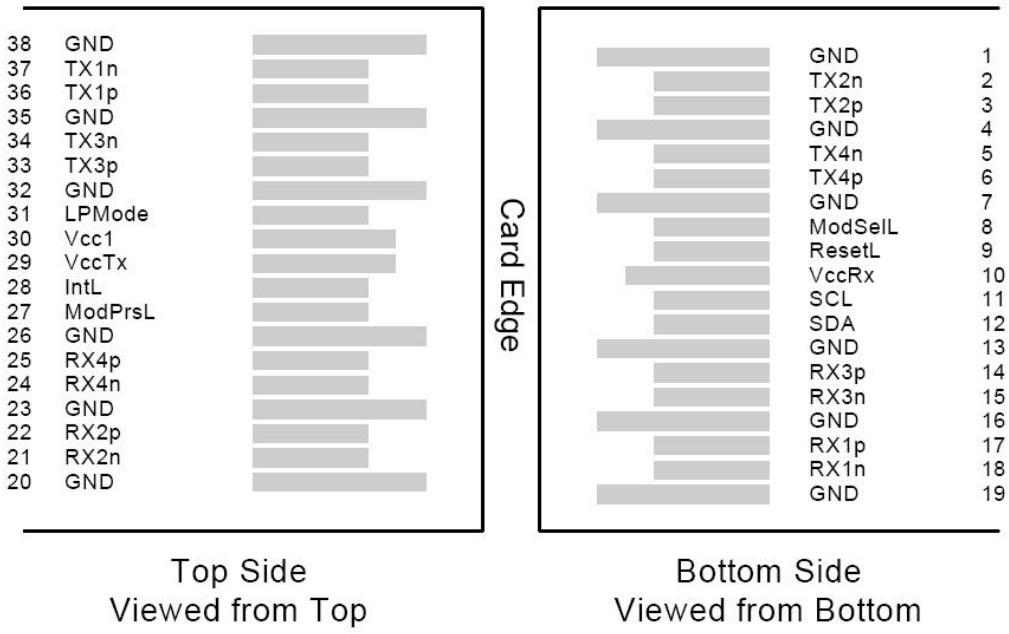

Figure3. QSFP Edge Connector and Pinout Description

QSFP Transceiver Pinout

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitted Inverted Data Input	3
3	CML-I	Tx2p	Transmitted Non-inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitted Inverted Data Input	3
6	CML-I	Tx4p	Transmitted Non-inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSeiL	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2
11	LVCMOS-I/O	SCL	Serial Clock for I^2C Interface	3
12	LVCMOS-I/O	SDA	Serial Data for I^2C Interface	3
13		GND	Ground	1

14	CML-O	RX3p	Receiver Non-inverted Data Output	3
15	CML-O	RX3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	RX1p	Receiver Non-inverted Data Output	3
18	CML-O	RX1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	RX2n	Receiver Inverted Data Output	3
22	CML-O	RX2p	Receiver Non-inverted Data Output	3
23		GND	Ground	1
24	CML-O	RX4n	Receiver Inverted Data Output	3
25	CML-O	RX4p	Receiver Non-inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2
30		Vcc1	+3.3 VDC Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	TX3p	Transmitted Non-inverted Data Input	3
34	CML-I	TX3n	Transmitted Inverted Data Input	3
35		GND	Ground	1
36	CML-I	TX1p	Transmitted Non-inverted Data Input	3
37	CML-I	TX1n	Transmitted Inverted Data Input	3
38		GND	Ground	1

Electrical Specifications - Low speed control signals

Host-QSFP Hardware pins description

There are 7 wires connected between the Host and the QSFP module. The signal levels and polarity are defined in the SFF-8436 standard.

TWS – (Two-wire serial interface) uses 2 signals namely: SCL (clock) and SDA (Data). The QSFP module Address is 50h='101000x'.
x='0' means write operation into QSFP, x='1' means read operation from QSFP.
The module responds to a TWS request only if the module is selected by the ModSelL pin. There are several read and write operation modes according to the standard and all of them are supported by QSFP module.

ModSelL – Module select pin. When low, the module responds to TWS communication.

ResetL – Reset pin. If ResetL ='0', the module initiates a complete reset routine which returns the module to default state settings. The routine starts only after ResetL is released (ResetL='1').

LPMode – Low Power Mode pin. When LPMode='1', the module power is reduced to below 1.5W. In this state, TWS

communication is operational, but the transmitter functionality is disabled. In addition, the LPMode can be controlled by software control bits. The software control bits are Power_over-ride and Power_set located in page LOWER MEMORY, Address byte 93 bits 0, 1 as shown in table below.

LPMode	Power_Overide Bit	Power_set Bit	Module Power Allowed
1	0	X	Low Power (< 1.5W)
0	0	X	High Power (< 3.5W)
X	1	1	Low Power (< 1.5W)
X	1	0	High Power (< 3.5W)

IntL – This is an output pin. When "LOW", the module indicates a possible module operational fault of a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

ModPrsL – This pin is pulled up to VCC at the host board and connected to ground in the module. The ModPrsL is asserted "LOW" when inserted and de-asserted "HIGH" when the module is physically absent from the host connector.

The timing parameters for the TWS interface to the QSFP module are shown below:

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	T_{LOW}	1.3		us	
Clock Pulse Width High	t_{HIGH}	0.6		us	
Time bus free before new transmission can start	t_{BUF}	20		us	Between STOP and START
START Hold Time	$t_{HD,STA}$	0.6		us	
START Set-up Time	$T_{SU,STA}$	0.6		us	
Data In Hold Time	$t_{HD,DTA}$	0		us	
Data In Set-up Time	$T_{SU,DTA}$	0.1		us	
Input Rise Time (400kHz)	$t_{R,400}$		300	ns	From (VIL,MAX-0.15) to (VIH,MIN+0.15)
Input Fall Time (400kHz)	$T_{F,400}$		300		From (VIH,MIN+0.15) to (VIL,MAX-0.15)
STOP Set-up Time	$T_{SU,STO}$	0.6		us	
ModSelL Setup Time	Host_select_setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	10		us	Delay from completion of a serial bus sequence to changes of transceiver select status
Aborted sequence-bus release	Deselect_Abort	2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence), to the QSFP module releasing SCL and SDA

Memory Interaction Specifications

QSFP Memory transaction timings and the Single and Multiple byte memory blocks are defined in the tables below.

Parameter	Symbol	Min	Max	Unit	
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	Maximum time the QSFP module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	t_{wr}		40	ms	Complete (up to) 4 Byte Write

When the host performs a write command, the SW first reads the bytes from the I^2C bus. Then, after the SW reaches the stop condition, the SW can write all the bytes. Following a write command, add at least a 16ms delay.

Mechanical Dimensions

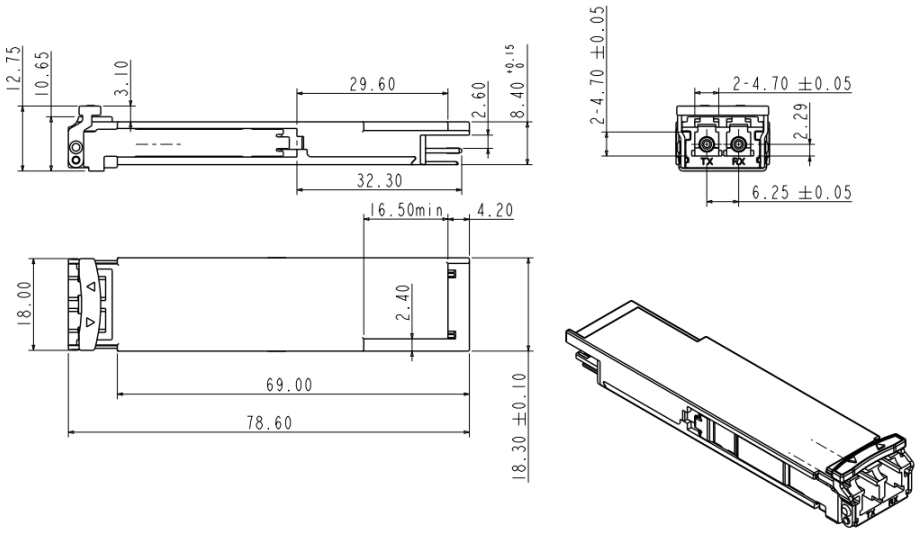

Figure4. Mechanical Specifications

Regulatory Compliance

Requirement	Standard
Electromagnetic Interference (EM)	Compliant to Class B requirements for FCC Part15 and CISPR 22
RF Immunity (RFI)	Compliant to EN/IEC 61000-4-3 and GR-1089-CORE Issue 4
Electrostatic Discharge (ESD)	Compliant to EN/IEC 61000-4-2 and GR-1089-CORE Issue 4 JEDEC JESD22-A114-B (2Kv limit)
Eye Safety	Compliant to Class 1M Laser Device per IEC60825-1
Lead Free Requirement (RoHS)	Compliant to 2002/95/EC RoHS 6/6 Directive

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