40G QSFP-8LC Connector Breakout AOC

Overview

APC QSFP+ to 8 x LC Connector Breakout Optical Cable are a high performance, low power consumption, long reach interconnect solution supporting 40G Ethernet, fiber channel and PCIe. It is compliant with the QSFP MSA and IEEE P802.3ba 40GBASE-SR4.

APC QSFP+ Breakout Cable is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 40Gb/s. QSFP+ Breakout Cable are suitable for short distances and offer a highly cost-effective way to connect within racks and across adjacent racks. These breakout cables connect to a 40G QSFP+ port of a switch on one end and to four 10G SFP+ Transceivers of a switch on the other end.

Features

♦ Full duplex 4CH 850nm parallel active optical cable
♦ Transmission data rate up to 10.3Gbit/s per channel
♦ SFF-8436 QSFP+ compliant
♦ Hot pluggable electrical interface
♦ Differential AC-coupled high speed data interface
♦ 4 channels 850nm VCSEL array
♦ 4 channels PIN photo detector array
♦ Maximum link length of 300m on OM3 Multimode Fiber (MMF) and 400m on OM4 MMF
♦ Low power consumption
♦ Housing isolated from connector ground
♦ Operating case temperature 0°C to +70°C
♦ 3.3V power supply voltage
♦ RoHS 6 compliant

Applications

♦ Infiniband transmission at 4ch SDR, DDR and QDR
♦ 40GBASE-SR4 40G Ethernet
♦ Data Centers

Ordering Information

Part Number	Product Description
AQS-40G-8LC-AOC-xx	40Gbps QSFP+ To 8LC Connectors, Active Optical Cable, 300m on OM3 MMF, 0ºC ~ +70ºC
XX : 01~300, 1~300Length in meters. (OM3 fiber is available)	

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd	2.5		10.3	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			1.5	W
Fiber Bend Radius	Rb	3			cm

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	180		1200	mVp-p
Differential output voltage amplitude	ΔVout	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BR			E-12	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note：
1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxNp and TxNn.
3. Differential output voltage amplitude is measured between RxNp and RxNn.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ_C	840	850	860	nm	-
RMS spectral width	$\Delta\lambda$	-	-	0.65	nm	-
Average launch power, each lane	Pout	-7.5	-	2.5	dBm	-
Difference in launch power between any two lanes (OMA)				4	dB	-
Extinction Ratio	ER	3	-	-	dB	-
Peak power, each lane				4	dBm	-
ransmitter and dispersion penalty (TDP), each lane	TDP			3.5	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4			Hit Ratio = 5x10-5	
Receiver						
Centre Wavelength	λ_C	840	850	860	nm	-
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm	1
Maximum Average power at receiver input, each lane				2.4	dBm	-
Receiver Reflectance				-12	dB	-
Peak power, each lane				4	dBm	-
LOS Assert		-30			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

Note：
1. Measured with conformance test signal at TP3 for BER = 10e-12

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	

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6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

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Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

Power Supply Filtering
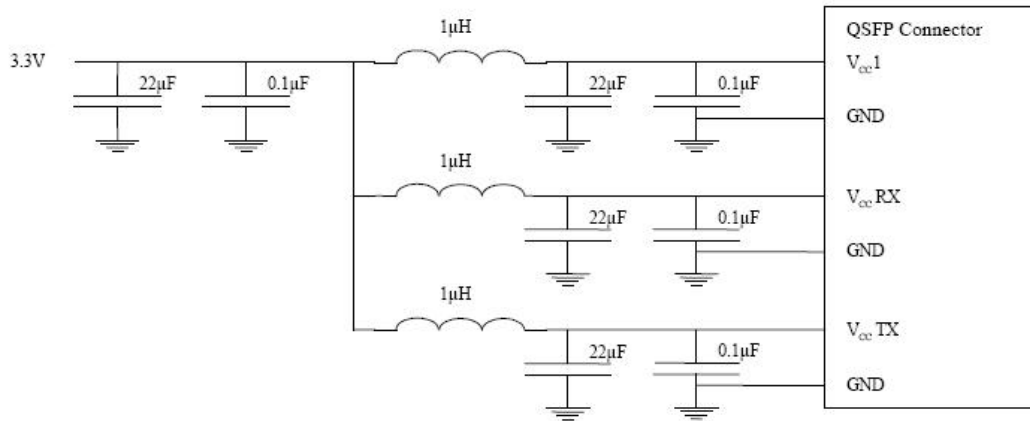The host board should use the power supply filtering shown in Figure3.

Figure1. Host Board Power Supply Filtering

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
LPMode Assert Time	ton_LPMode	100	µs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted

Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional3

Note：

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.
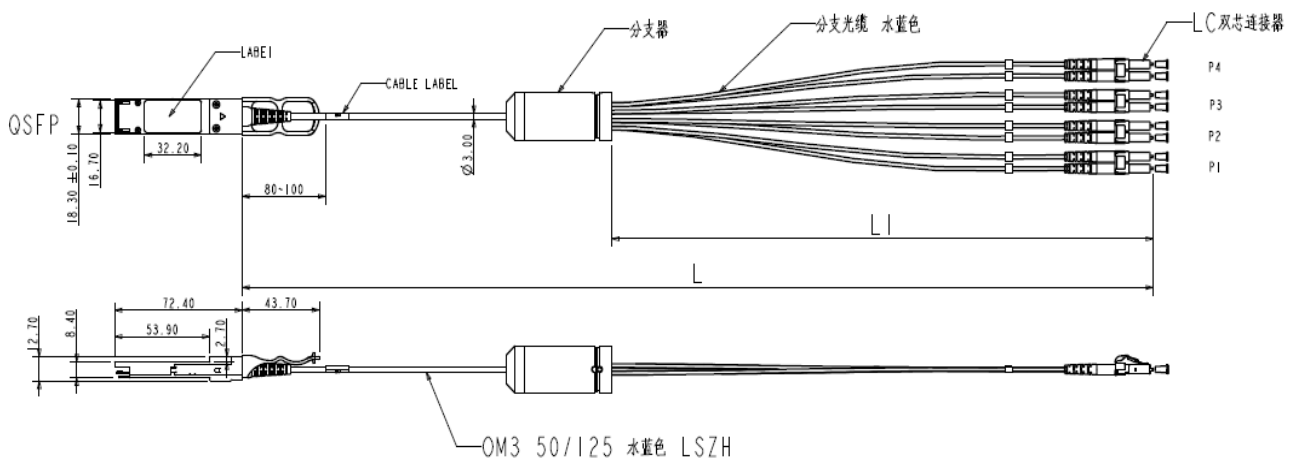
Mechanical Dimensions

Figure2. Mechanical Specifications

References

1. SFF-8436 QSFP+
2. Infiniband IB-4x-SX, IB-4x-DDR-SX, IB-4x-QDR-SX
3. Ethernet 40GBASE-SR4